

-

PCH\_GPI0

Function	Pin No.	Signal Name	IO Type	IO Mode
GPIO0_0	1	GPIO0_0	Output	Push-Pull
GPIO0_1	2	GPIO0_1	Output	Push-Pull
GPIO0_2	3	GPIO0_2	Output	Push-Pull
GPIO0_3	4	GPIO0_3	Output	Push-Pull
GPIO0_4	5	GPIO0_4	Output	Push-Pull
GPIO0_5	6	GPIO0_5	Output	Push-Pull
GPIO0_6	7	GPIO0_6	Output	Push-Pull
GPIO0_7	8	GPIO0_7	Output	Push-Pull
GPIO0_8	9	GPIO0_8	Output	Push-Pull
GPIO0_9	10	GPIO0_9	Output	Push-Pull
GPIO0_10	11	GPIO0_10	Output	Push-Pull
GPIO0_11	12	GPIO0_11	Output	Push-Pull
GPIO0_12	13	GPIO0_12	Output	Push-Pull
GPIO0_13	14	GPIO0_13	Output	Push-Pull
GPIO0_14	15	GPIO0_14	Output	Push-Pull
GPIO0_15	16	GPIO0_15	Output	Push-Pull
GPIO0_16	17	GPIO0_16	Output	Push-Pull
GPIO0_17	18	GPIO0_17	Output	Push-Pull
GPIO0_18	19	GPIO0_18	Output	Push-Pull
GPIO0_19	20	GPIO0_19	Output	Push-Pull
GPIO0_20	21	GPIO0_20	Output	Push-Pull
GPIO0_21	22	GPIO0_21	Output	Push-Pull
GPIO0_22	23	GPIO0_22	Output	Push-Pull
GPIO0_23	24	GPIO0_23	Output	Push-Pull
GPIO0_24	25	GPIO0_24	Output	Push-Pull
GPIO0_25	26	GPIO0_25	Output	Push-Pull
GPIO0_26	27	GPIO0_26	Output	Push-Pull
GPIO0_27	28	GPIO0_27	Output	Push-Pull
GPIO0_28	29	GPIO0_28	Output	Push-Pull
GPIO0_29	30	GPIO0_29	Output	Push-Pull
GPIO0_30	31	GPIO0_30	Output	Push-Pull

Function	Pin No.	Signal Name	IO Type	IO Mode
GPIO1_0	32	GPIO1_0	Output	Push-Pull
GPIO1_1	33	GPIO1_1	Output	Push-Pull
GPIO1_2	34	GPIO1_2	Output	Push-Pull
GPIO1_3	35	GPIO1_3	Output	Push-Pull
GPIO1_4	36	GPIO1_4	Output	Push-Pull
GPIO1_5	37	GPIO1_5	Output	Push-Pull
GPIO1_6	38	GPIO1_6	Output	Push-Pull
GPIO1_7	39	GPIO1_7	Output	Push-Pull
GPIO1_8	40	GPIO1_8	Output	Push-Pull
GPIO1_9	41	GPIO1_9	Output	Push-Pull
GPIO1_10	42	GPIO1_10	Output	Push-Pull
GPIO1_11	43	GPIO1_11	Output	Push-Pull
GPIO1_12	44	GPIO1_12	Output	Push-Pull
GPIO1_13	45	GPIO1_13	Output	Push-Pull
GPIO1_14	46	GPIO1_14	Output	Push-Pull
GPIO1_15	47	GPIO1_15	Output	Push-Pull
GPIO1_16	48	GPIO1_16	Output	Push-Pull
GPIO1_17	49	GPIO1_17	Output	Push-Pull
GPIO1_18	50	GPIO1_18	Output	Push-Pull
GPIO1_19	51	GPIO1_19	Output	Push-Pull
GPIO1_20	52	GPIO1_20	Output	Push-Pull
GPIO1_21	53	GPIO1_21	Output	Push-Pull
GPIO1_22	54	GPIO1_22	Output	Push-Pull
GPIO1_23	55	GPIO1_23	Output	Push-Pull
GPIO1_24	56	GPIO1_24	Output	Push-Pull
GPIO1_25	57	GPIO1_25	Output	Push-Pull
GPIO1_26	58	GPIO1_26	Output	Push-Pull
GPIO1_27	59	GPIO1_27	Output	Push-Pull
GPIO1_28	60	GPIO1_28	Output	Push-Pull
GPIO1_29	61	GPIO1_29	Output	Push-Pull
GPIO1_30	62	GPIO1_30	Output	Push-Pull
GPIO1_31	63	GPIO1_31	Output	Push-Pull

EC17B95 GPIO

Function	Pin No.	Signal Name	IO Type	IO Mode
GPIO2_0	64	GPIO2_0	Output	Push-Pull
GPIO2_1	65	GPIO2_1	Output	Push-Pull
GPIO2_2	66	GPIO2_2	Output	Push-Pull
GPIO2_3	67	GPIO2_3	Output	Push-Pull
GPIO2_4	68	GPIO2_4	Output	Push-Pull
GPIO2_5	69	GPIO2_5	Output	Push-Pull
GPIO2_6	70	GPIO2_6	Output	Push-Pull
GPIO2_7	71	GPIO2_7	Output	Push-Pull
GPIO2_8	72	GPIO2_8	Output	Push-Pull
GPIO2_9	73	GPIO2_9	Output	Push-Pull
GPIO2_10	74	GPIO2_10	Output	Push-Pull
GPIO2_11	75	GPIO2_11	Output	Push-Pull
GPIO2_12	76	GPIO2_12	Output	Push-Pull
GPIO2_13	77	GPIO2_13	Output	Push-Pull
GPIO2_14	78	GPIO2_14	Output	Push-Pull
GPIO2_15	79	GPIO2_15	Output	Push-Pull
GPIO2_16	80	GPIO2_16	Output	Push-Pull
GPIO2_17	81	GPIO2_17	Output	Push-Pull
GPIO2_18	82	GPIO2_18	Output	Push-Pull
GPIO2_19	83	GPIO2_19	Output	Push-Pull
GPIO2_20	84	GPIO2_20	Output	Push-Pull
GPIO2_21	85	GPIO2_21	Output	Push-Pull
GPIO2_22	86	GPIO2_22	Output	Push-Pull
GPIO2_23	87	GPIO2_23	Output	Push-Pull
GPIO2_24	88	GPIO2_24	Output	Push-Pull
GPIO2_25	89	GPIO2_25	Output	Push-Pull
GPIO2_26	90	GPIO2_26	Output	Push-Pull
GPIO2_27	91	GPIO2_27	Output	Push-Pull
GPIO2_28	92	GPIO2_28	Output	Push-Pull
GPIO2_29	93	GPIO2_29	Output	Push-Pull
GPIO2_30	94	GPIO2_30	Output	Push-Pull
GPIO2_31	95	GPIO2_31	Output	Push-Pull

GL7250W Setting

Function	Pin No.	Signal Name	IO Type	IO Mode
GPIO3_0	96	GPIO3_0	Output	Push-Pull
GPIO3_1	97	GPIO3_1	Output	Push-Pull
GPIO3_2	98	GPIO3_2	Output	Push-Pull
GPIO3_3	99	GPIO3_3	Output	Push-Pull
GPIO3_4	100	GPIO3_4	Output	Push-Pull
GPIO3_5	101	GPIO3_5	Output	Push-Pull
GPIO3_6	102	GPIO3_6	Output	Push-Pull
GPIO3_7	103	GPIO3_7	Output	Push-Pull
GPIO3_8	104	GPIO3_8	Output	Push-Pull
GPIO3_9	105	GPIO3_9	Output	Push-Pull
GPIO3_10	106	GPIO3_10	Output	Push-Pull
GPIO3_11	107	GPIO3_11	Output	Push-Pull
GPIO3_12	108	GPIO3_12	Output	Push-Pull
GPIO3_13	109	GPIO3_13	Output	Push-Pull
GPIO3_14	110	GPIO3_14	Output	Push-Pull
GPIO3_15	111	GPIO3_15	Output	Push-Pull
GPIO3_16	112	GPIO3_16	Output	Push-Pull
GPIO3_17	113	GPIO3_17	Output	Push-Pull
GPIO3_18	114	GPIO3_18	Output	Push-Pull
GPIO3_19	115	GPIO3_19	Output	Push-Pull
GPIO3_20	116	GPIO3_20	Output	Push-Pull
GPIO3_21	117	GPIO3_21	Output	Push-Pull
GPIO3_22	118	GPIO3_22	Output	Push-Pull
GPIO3_23	119	GPIO3_23	Output	Push-Pull
GPIO3_24	120	GPIO3_24	Output	Push-Pull
GPIO3_25	121	GPIO3_25	Output	Push-Pull
GPIO3_26	122	GPIO3_26	Output	Push-Pull
GPIO3_27	123	GPIO3_27	Output	Push-Pull
GPIO3_28	124	GPIO3_28	Output	Push-Pull
GPIO3_29	125	GPIO3_29	Output	Push-Pull
GPIO3_30	126	GPIO3_30	Output	Push-Pull
GPIO3_31	127	GPIO3_31	Output	Push-Pull

Function	Pin No.	Signal Name	IO Type	IO Mode
GPIO4_0	128	GPIO4_0	Output	Push-Pull
GPIO4_1	129	GPIO4_1	Output	Push-Pull
GPIO4_2	130	GPIO4_2	Output	Push-Pull
GPIO4_3	131	GPIO4_3	Output	Push-Pull
GPIO4_4	132	GPIO4_4	Output	Push-Pull
GPIO4_5	133	GPIO4_5	Output	Push-Pull
GPIO4_6	134	GPIO4_6	Output	Push-Pull
GPIO4_7	135	GPIO4_7	Output	Push-Pull
GPIO4_8	136	GPIO4_8	Output	Push-Pull
GPIO4_9	137	GPIO4_9	Output	Push-Pull
GPIO4_10	138	GPIO4_10	Output	Push-Pull
GPIO4_11	139	GPIO4_11	Output	Push-Pull
GPIO4_12	140	GPIO4_12	Output	Push-Pull
GPIO4_13	141	GPIO4_13	Output	Push-Pull
GPIO4_14	142	GPIO4_14	Output	Push-Pull
GPIO4_15	143	GPIO4_15	Output	Push-Pull
GPIO4_16	144	GPIO4_16	Output	Push-Pull
GPIO4_17	145	GPIO4_17	Output	Push-Pull
GPIO4_18	146	GPIO4_18	Output	Push-Pull
GPIO4_19	147	GPIO4_19	Output	Push-Pull
GPIO4_20	148	GPIO4_20	Output	Push-Pull
GPIO4_21	149	GPIO4_21	Output	Push-Pull
GPIO4_22	150	GPIO4_22	Output	Push-Pull
GPIO4_23	151	GPIO4_23	Output	Push-Pull
GPIO4_24	152	GPIO4_24	Output	Push-Pull
GPIO4_25	153	GPIO4_25	Output	Push-Pull
GPIO4_26	154	GPIO4_26	Output	Push-Pull
GPIO4_27	155	GPIO4_27	Output	Push-Pull
GPIO4_28	156	GPIO4_28	Output	Push-Pull
GPIO4_29	157	GPIO4_29	Output	Push-Pull
GPIO4_30	158	GPIO4_30	Output	Push-Pull
GPIO4_31	159	GPIO4_31	Output	Push-Pull

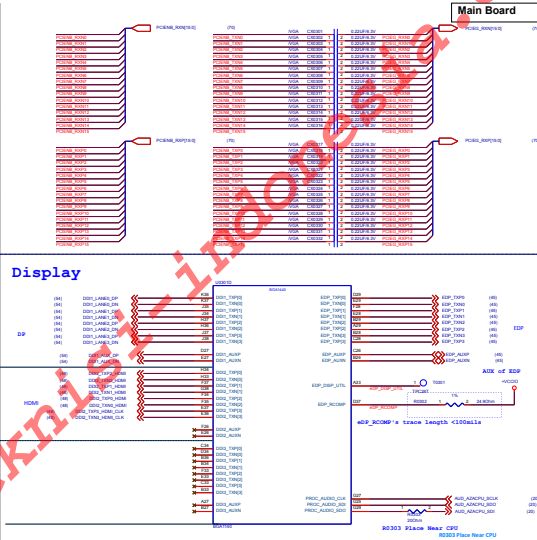
Function	Pin No.	Signal Name	IO Type	IO Mode
GPIO5_0	160	GPIO5_0	Output	Push-Pull
GPIO5_1	161	GPIO5_1	Output	Push-Pull
GPIO5_2	162	GPIO5_2	Output	Push-Pull
GPIO5_3	163	GPIO5_3	Output	Push-Pull
GPIO5_4	164	GPIO5_4	Output	Push-Pull
GPIO5_5	165	GPIO5_5	Output	Push-Pull
GPIO5_6	166	GPIO5_6	Output	Push-Pull
GPIO5_7	167	GPIO5_7	Output	Push-Pull
GPIO5_8	168	GPIO5_8	Output	Push-Pull
GPIO5_9	169	GPIO5_9	Output	Push-Pull
GPIO5_10	170	GPIO5_10	Output	Push-Pull
GPIO5_11	171	GPIO5_11	Output	Push-Pull
GPIO5_12	172	GPIO5_12	Output	Push-Pull
GPIO5_13	173	GPIO5_13	Output	Push-Pull
GPIO5_14	174	GPIO5_14	Output	Push-Pull
GPIO5_15	175	GPIO5_15	Output	Push-Pull
GPIO5_16	176	GPIO5_16	Output	Push-Pull
GPIO5_17	177	GPIO5_17	Output	Push-Pull
GPIO5_18	178	GPIO5_18	Output	Push-Pull
GPIO5_19	179	GPIO5_19	Output	Push-Pull
GPIO5_20	180	GPIO5_20	Output	Push-Pull
GPIO5_21	181	GPIO5_21	Output	Push-Pull
GPIO5_22	182	GPIO5_22	Output	Push-Pull
GPIO5_23	183	GPIO5_23	Output	Push-Pull
GPIO5_24	184	GPIO5_24	Output	Push-Pull
GPIO5_25	185	GPIO5_25	Output	Push-Pull
GPIO5_26	186	GPIO5_26	Output	Push-Pull
GPIO5_27	187	GPIO5_27	Output	Push-Pull
GPIO5_28	188	GPIO5_28	Output	Push-Pull
GPIO5_29	189	GPIO5_29	Output	Push-Pull
GPIO5_30	190	GPIO5_30	Output	Push-Pull
GPIO5_31	191	GPIO5_31	Output	Push-Pull

Function	Pin No.	Signal Name	IO Type	IO Mode
GPIO6_0	192	GPIO6_0	Output	Push-Pull
GPIO6_1	193	GPIO6_1	Output	Push-Pull
GPIO6_2	194	GPIO6_2	Output	Push-Pull
GPIO6_3	195	GPIO6_3	Output	Push-Pull
GPIO6_4	196	GPIO6_4	Output	Push-Pull
GPIO6_5	197	GPIO6_5	Output	Push-Pull
GPIO6_6	198	GPIO6_6	Output	Push-Pull
GPIO6_7	199	GPIO6_7	Output	Push-Pull
GPIO6_8	200	GPIO6_8	Output	Push-Pull
GPIO6_9	201	GPIO6_9	Output	Push-Pull
GPIO6_10	202	GPIO6_10	Output	Push-Pull
GPIO6_11	203	GPIO6_11	Output	Push-Pull
GPIO6_12	204	GPIO6_12	Output	Push-Pull
GPIO6_13	205	GPIO6_13	Output	Push-Pull
GPIO6_14	206	GPIO6_14	Output	Push-Pull
GPIO6_15	207	GPIO6_15	Output	Push-Pull
GPIO6_16	208	GPIO6_16	Output	Push-Pull
GPIO6_17	209	GPIO6_17	Output	Push-Pull
GPIO6_18	210	GPIO6_18	Output	Push-Pull
GPIO6_19	211	GPIO6_19	Output	Push-Pull
GPIO6_20	212	GPIO6_20	Output	Push-Pull
GPIO6_21	213	GPIO6_21	Output	Push-Pull
GPIO6_22	214	GPIO6_22	Output	Push-Pull
GPIO6_23	215	GPIO6_23	Output	Push-Pull
GPIO6_24	216	GPIO6_24	Output	Push-Pull
GPIO6_25	217	GPIO6_25	Output	Push-Pull
GPIO6_26	218	GPIO6_26	Output	Push-Pull
GPIO6_27	219	GPIO6_27	Output	Push-Pull
GPIO6_28	220	GPIO6_28	Output	Push-Pull
GPIO6_29	221	GPIO6_29	Output	Push-Pull
GPIO6_30	222	GPIO6_30	Output	Push-Pull
GPIO6_31	223	GPIO6_31	Output	Push-Pull

# PCIEG

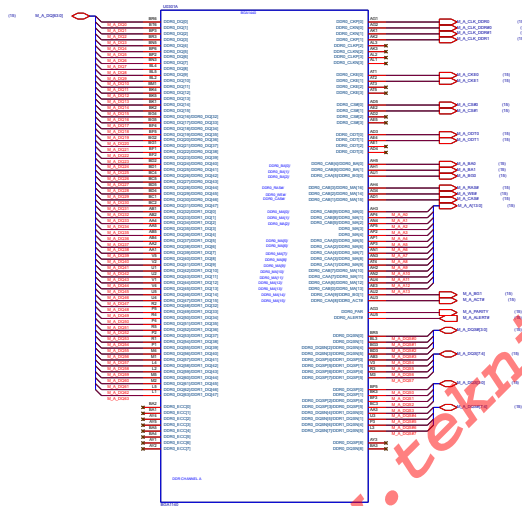
EDS 544924  
Table 2-17

Rev 1.25

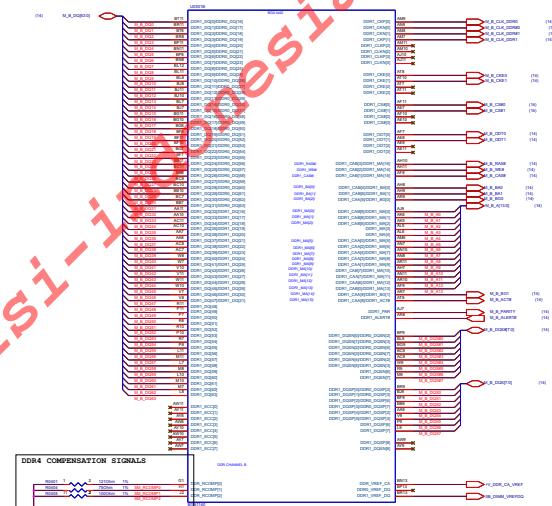


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# Memory Channel A

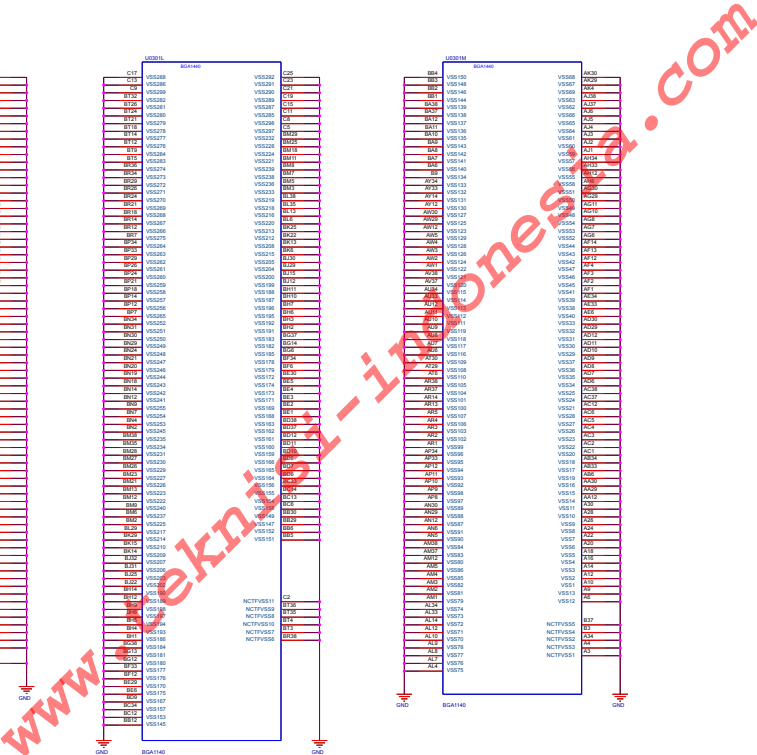
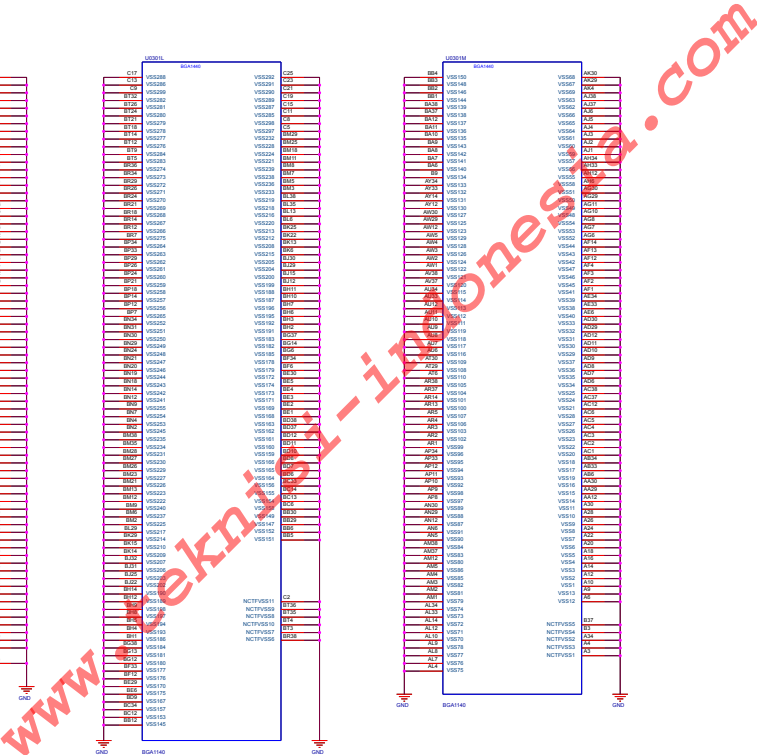


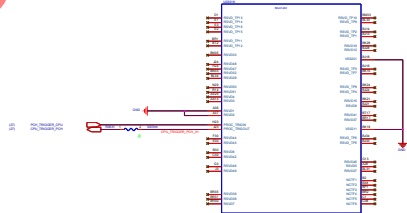
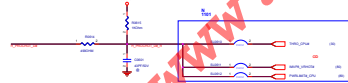
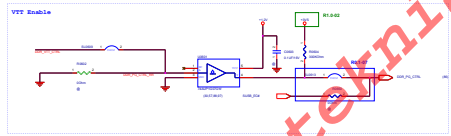
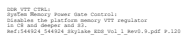
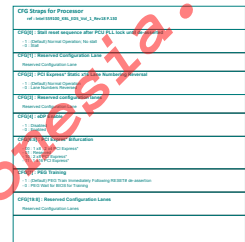
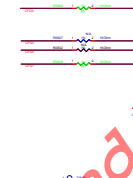
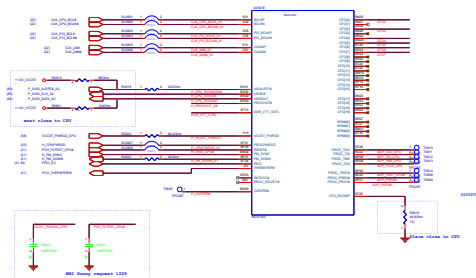
# Memory Channel B

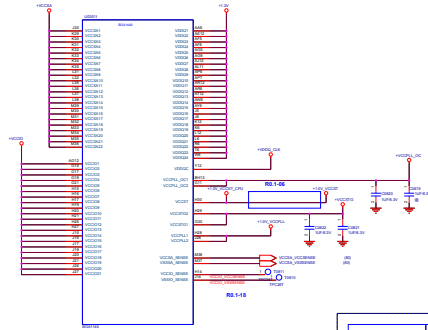


# Main Board





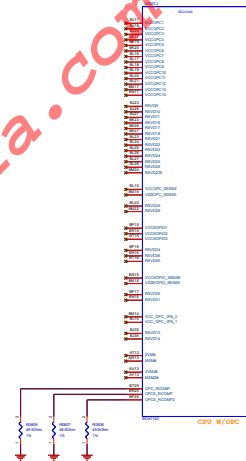




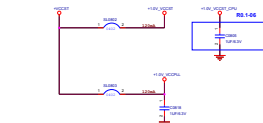
Main Source	1st PWR	2nd PWR	3rd PWR
AC Decaps	+1.0V_VDDQ	+VDDQ	+1.0V_VDDQ
	+1.0V_VDDQ	+VDDQ	+1.0V_VDDQ
	+1.0V_VDDQ	+VDDQ	+1.0V_VDDQ
	+1.0V_VDDQ	+VDDQ	+1.0V_VDDQ
	+VDDQ	+VDDQ	+VDDQ
	+VDDQ	+VDDQ	+VDDQ

## OPC Power Rails

## Main Board



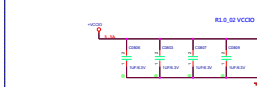
## +1.0V\_VDDQ/+1.0V\_VDDQ



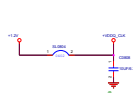
## +VDDQ DECAPS Place Back Side (TOP)



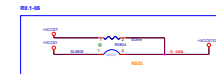
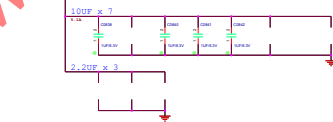
## +VDDQ DECAPS Place Back Side (TOP)



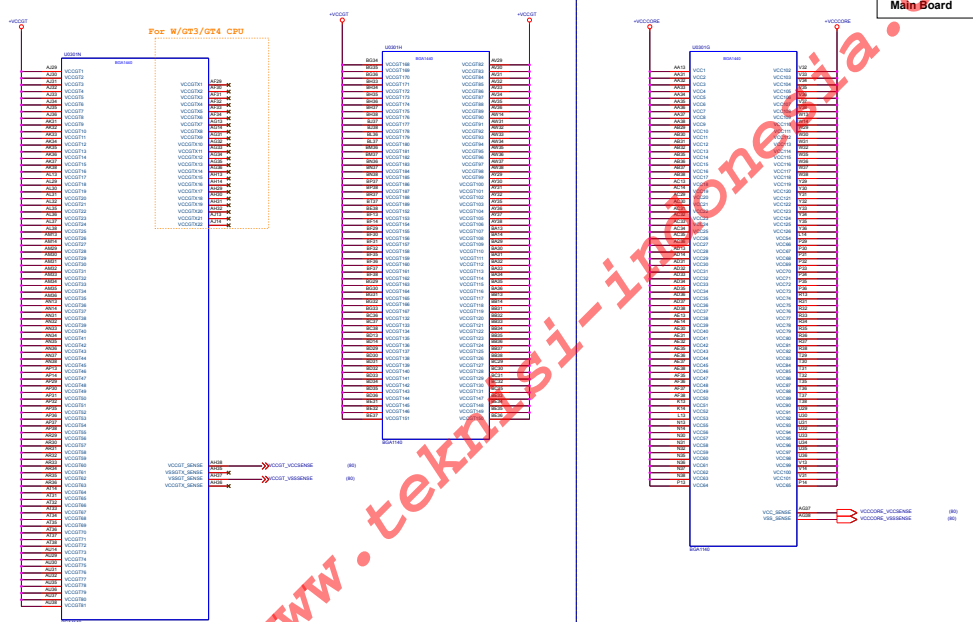
## +VDDQ\_CLK DECAPS Place Back Side (TOP)



## +VDDQ DECAPS Place Back Side (TOP)

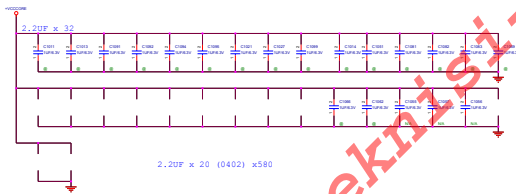
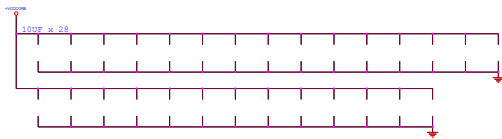


Volume Segment:  
+VDDQ is supplied +1.0V (shared with +VDDQ)

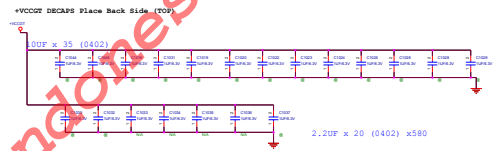




\*VCCORE DECAPS Place Back Side (TOP)

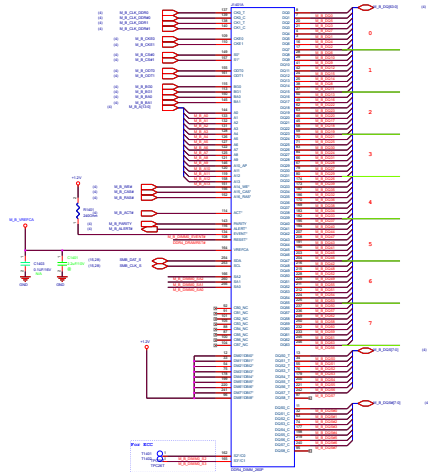


\*VCC02 DECAPS Place Back Side (TOP)



Main Board

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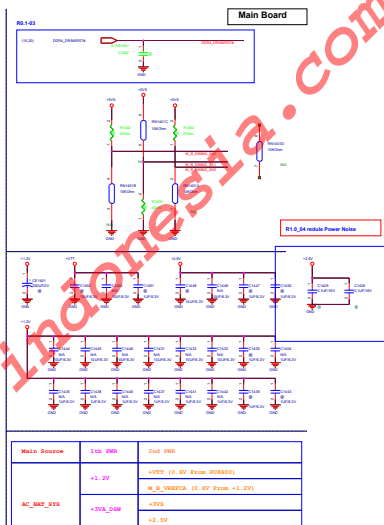
[illegible]

```

HD-DIMMs that do not support XDC (add only) will
use the XPC with XDC#N not wired.
HD-DIMMs that support XDC (x86) will use a
combined XPC/Thermal Sensor with XDC#N wired.

                                DIMM_OVRD_XPC
XDC#N#N ON HD-DIMM: XDC#N will UP IF NO PIN IN P

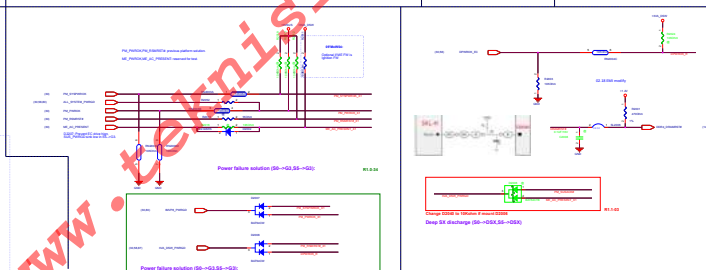
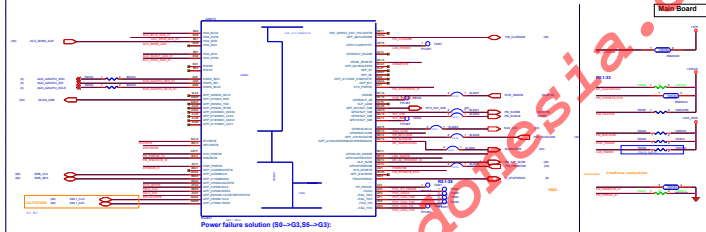
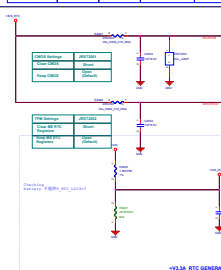
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[illegible]

Block Name	1st FIB	2nd FIB	3rd FIB	6th
+PCBMT	+PCB_MBT	+PCB_MBT		
AC_RST_FIB	+1.00000	+00000	+1.00_00000	
	+1.20			
	+FIB0	+FIB	+FIB_M0	
		+PCBMT	+PCB_MBT	+PCB_MBT00
	+FIB_000	+FIB		



# PCIE Setting

PCIE Function define  
KabyLake HMT5

Function	Device	Vendor	Model	Manufacturer
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0000:00:00.1	0000:00:00.1	0000:00:00.1	0000:00:00.1	0000:00:00.1
0000:00:00.2	0000:00:00.2	0000:00:00.2	0000:00:00.2	0000:00:00.2
0000:00:00.3	0000:00:00.3	0000:00:00.3	0000:00:00.3	0000:00:00.3
0000:00:00.4	0000:00:00.4	0000:00:00.4	0000:00:00.4	0000:00:00.4
0000:00:00.5	0000:00:00.5	0000:00:00.5	0000:00:00.5	0000:00:00.5
0000:00:00.6	0000:00:00.6	0000:00:00.6	0000:00:00.6	0000:00:00.6
0000:00:00.7	0000:00:00.7	0000:00:00.7	0000:00:00.7	0000:00:00.7
0000:00:00.8	0000:00:00.8	0000:00:00.8	0000:00:00.8	0000:00:00.8
0000:00:00.9	0000:00:00.9	0000:00:00.9	0000:00:00.9	0000:00:00.9
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0000:00:00.13	0000:00:00.13	0000:00:00.13	0000:00:00.13	0000:00:00.13
0000:00:00.14	0000:00:00.14	0000:00:00.14	0000:00:00.14	0000:00:00.14
0000:00:00.15	0000:00:00.15	0000:00:00.15	0000:00:00.15	0000:00:00.15
0000:00:00.16	0000:00:00.16	0000:00:00.16	0000:00:00.16	0000:00:00.16
0000:00:00.17	0000:00:00.17	0000:00:00.17	0000:00:00.17	0000:00:00.17
0000:00:00.18	0000:00:00.18	0000:00:00.18	0000:00:00.18	0000:00:00.18
0000:00:00.19	0000:00:00.19	0000:00:00.19	0000:00:00.19	0000:00:00.19
0000:00:00.1A	0000:00:00.1A	0000:00:00.1A	0000:00:00.1A	0000:00:00.1A
0000:00:00.1B	0000:00:00.1B	0000:00:00.1B	0000:00:00.1B	0000:00:00.1B
0000:00:00.1C	0000:00:00.1C	0000:00:00.1C	0000:00:00.1C	0000:00:00.1C
0000:00:00.1D	0000:00:00.1D	0000:00:00.1D	0000:00:00.1D	0000:00:00.1D
0000:00:00.1E	0000:00:00.1E	0000:00:00.1E	0000:00:00.1E	0000:00:00.1E
0000:00:00.1F	0000:00:00.1F	0000:00:00.1F	0000:00:00.1F	0000:00:00.1F

## X1800D USB Function define

KabyLake HMT5

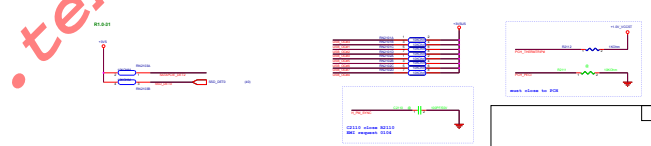
### USB Setting

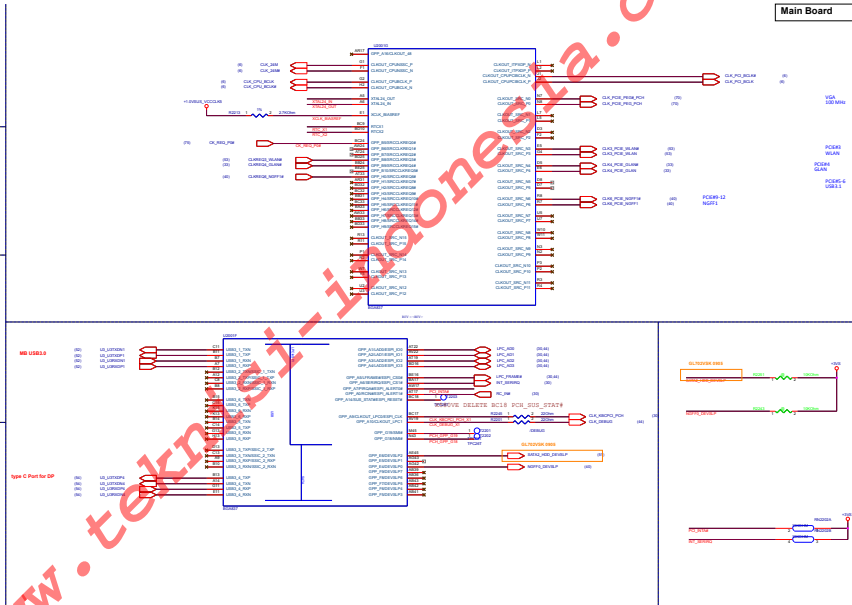
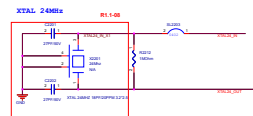
USB ID	Function	USB ID	Function
USB0_0	USB0_0 (USB0_0)	USB0_0	USB0_0
USB0_1	USB0_1 (USB0_1)	USB0_1	USB0_1
USB0_2	USB0_2 (USB0_2)	USB0_2	USB0_2
USB0_3	USB0_3 (USB0_3)	USB0_3	USB0_3
USB0_4	USB0_4 (USB0_4)	USB0_4	USB0_4
USB0_5	USB0_5 (USB0_5)	USB0_5	USB0_5
USB0_6	USB0_6 (USB0_6)	USB0_6	USB0_6
USB0_7	USB0_7 (USB0_7)	USB0_7	USB0_7
USB0_8	USB0_8 (USB0_8)	USB0_8	USB0_8
USB0_9	USB0_9 (USB0_9)	USB0_9	USB0_9
USB0_A	USB0_A (USB0_A)	USB0_A	USB0_A
USB0_B	USB0_B (USB0_B)	USB0_B	USB0_B
USB0_C	USB0_C (USB0_C)	USB0_C	USB0_C
USB0_D	USB0_D (USB0_D)	USB0_D	USB0_D
USB0_E	USB0_E (USB0_E)	USB0_E	USB0_E
USB0_F	USB0_F (USB0_F)	USB0_F	USB0_F
USB0_10	USB0_10 (USB0_10)	USB0_10	USB0_10
USB0_11	USB0_11 (USB0_11)	USB0_11	USB0_11
USB0_12	USB0_12 (USB0_12)	USB0_12	USB0_12
USB0_13	USB0_13 (USB0_13)	USB0_13	USB0_13
USB0_14	USB0_14 (USB0_14)	USB0_14	USB0_14
USB0_15	USB0_15 (USB0_15)	USB0_15	USB0_15

## X1800D PCIE/DATA Function define

PCIE ID	Function	PCIE ID	Function
PCIE_0	PCIE_0 (PCIE_0)	PCIE_0	PCIE_0
PCIE_1	PCIE_1 (PCIE_1)	PCIE_1	PCIE_1
PCIE_2	PCIE_2 (PCIE_2)	PCIE_2	PCIE_2
PCIE_3	PCIE_3 (PCIE_3)	PCIE_3	PCIE_3
PCIE_4	PCIE_4 (PCIE_4)	PCIE_4	PCIE_4
PCIE_5	PCIE_5 (PCIE_5)	PCIE_5	PCIE_5
PCIE_6	PCIE_6 (PCIE_6)	PCIE_6	PCIE_6
PCIE_7	PCIE_7 (PCIE_7)	PCIE_7	PCIE_7
PCIE_8	PCIE_8 (PCIE_8)	PCIE_8	PCIE_8
PCIE_9	PCIE_9 (PCIE_9)	PCIE_9	PCIE_9
PCIE_A	PCIE_A (PCIE_A)	PCIE_A	PCIE_A
PCIE_B	PCIE_B (PCIE_B)	PCIE_B	PCIE_B
PCIE_C	PCIE_C (PCIE_C)	PCIE_C	PCIE_C
PCIE_D	PCIE_D (PCIE_D)	PCIE_D	PCIE_D
PCIE_E	PCIE_E (PCIE_E)	PCIE_E	PCIE_E
PCIE_F	PCIE_F (PCIE_F)	PCIE_F	PCIE_F

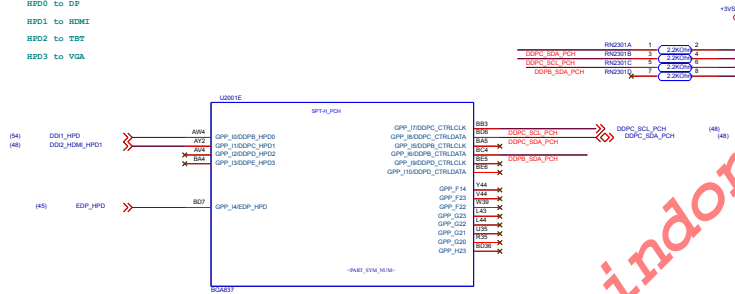
PCIE ID	Function
PCIE_0	PCIE_0
PCIE_1	PCIE_1
PCIE_2	PCIE_2
PCIE_3	PCIE_3
PCIE_4	PCIE_4
PCIE_5	PCIE_5
PCIE_6	PCIE_6
PCIE_7	PCIE_7
PCIE_8	PCIE_8
PCIE_9	PCIE_9
PCIE_A	PCIE_A
PCIE_B	PCIE_B
PCIE_C	PCIE_C
PCIE_D	PCIE_D
PCIE_E	PCIE_E
PCIE_F	PCIE_F





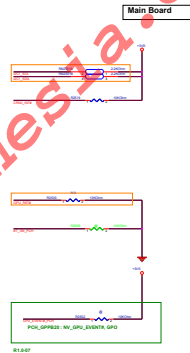
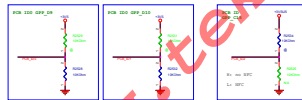
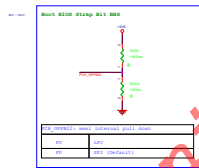
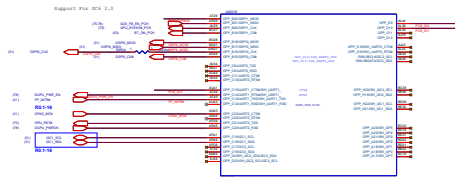
## Main Board

```
HPD0 to DP
HPD1 to HDMI
HPD2 to TBT
HPD3 to VGA
```

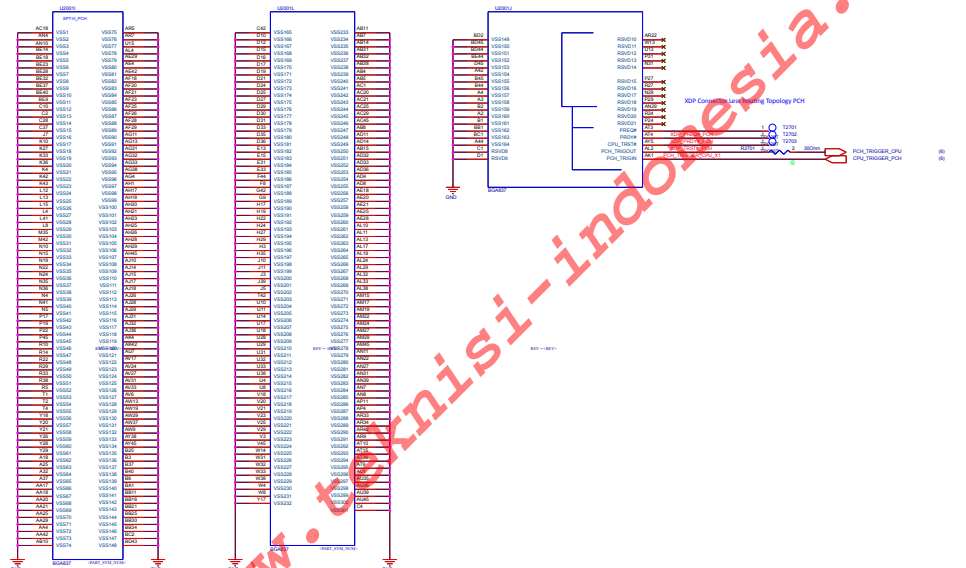

$$25V = -25V$$



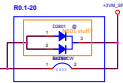






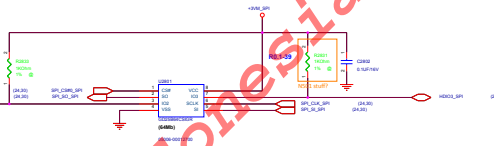


## SPI Power



## 1st SPI ROM

Main: 05006-00010500 (Fixed quad bit)



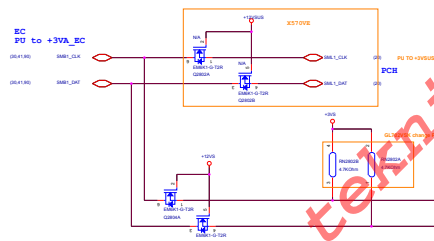
Main Board

## System Management Interface

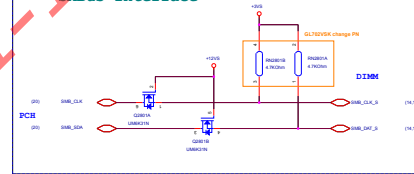
EC  
PU to +3VA\_EC

(SMB.LIN)

(SMB.LIN)



## SMBus Interface



R5.1-13 R1.0-01

CPU, VGA Thermal Sensor  
Power Thermal Sensor

<b>SC 8995</b> <b>Only 3V Tolerance</b> (SPC1, S2, S3, S4, S5, S6) (SPC1, S2, S3, S4, S5, S6) (SPC1, S2, S3, S4, S5, S6) (SPC1, S2, S3, S4, S5, S6) (SPC1, S2, S3, S4, S5, S6) (SPC1, S2, S3, S4, S5, S6) (SPC1, S2, S3, S4, S5, S6) (SPC1, S2, S3, S4, S5, S6)	<b>SC Require</b>
--	-------------------

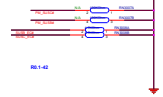
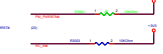
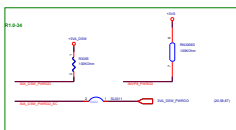
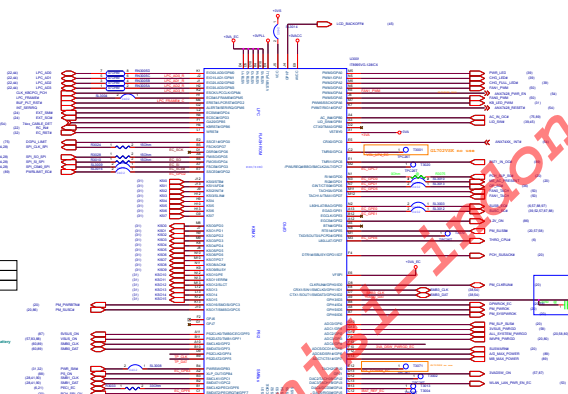
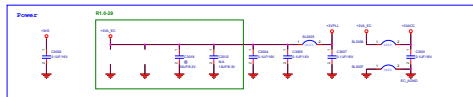
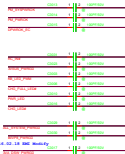
Data be adjusted to  
Open-Drain for part.

(SPC1, S2, S3, S4, S5, S6)  
 (SPC1, S2, S3, S4, S5, S6)  
 (SPC1, S2, S3, S4, S5, S6)  
 (SPC1, S2, S3, S4, S5, S6)  
 (SPC1, S2, S3, S4, S5, S6)  
 (SPC1, S2, S3, S4, S5, S6)  
 (SPC1, S2, S3, S4, S5, S6)  
 (SPC1, S2, S3, S4, S5, S6)

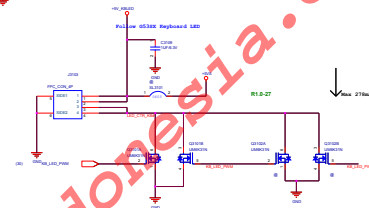
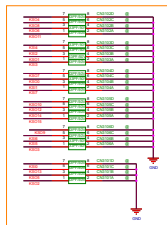
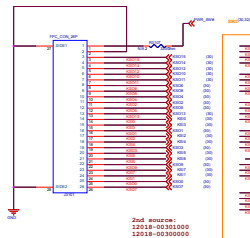
<b>IDE Version</b> 1999/09/09	<b>ADU P/M</b> 00000000000000000000
----------------------------------	--

2010.08.21.00000000000000000000

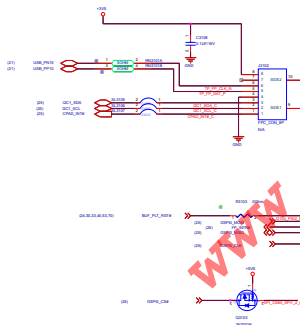
For EMI



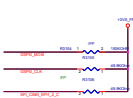
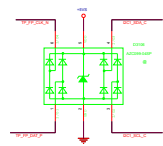
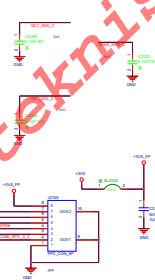
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Click touch Pad Connector



Reserved for EMI



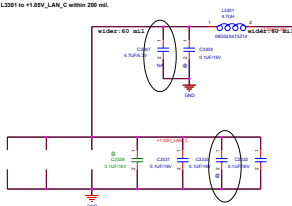
Full up: +VDD through K7907(100nA) to +VDDnA  
When +VDD ready, K7907(100nA) and K3006(7.5nA) will be in passCis.  
The CPU temperature point is protected ahead of time.  
Information +VDD3 output can output to +VDD3 K0034



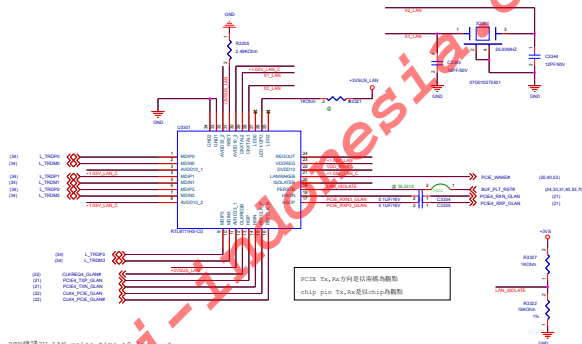
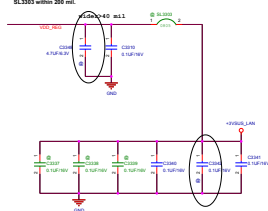
Main Board

The distance from u3301.36 to L3301 within 200 mil.

The distance from L3301 to +1.85V\_LAN\_C within 200 mil.



The distance from L3301.36, U3301.36, VDD\_REG net to SL3303 within 200 mil.



RTK建議TV\_LAN raise time >0.5uS

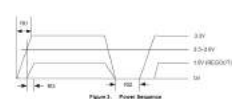
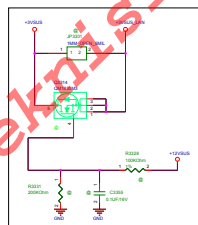


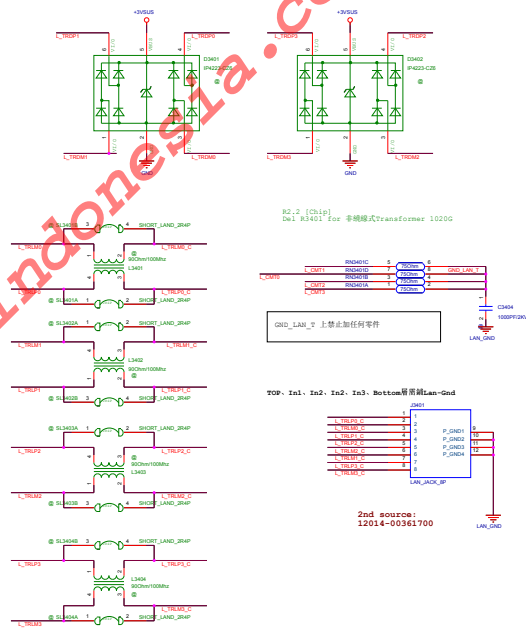
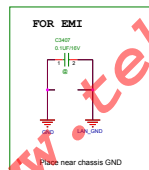
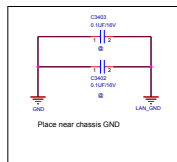
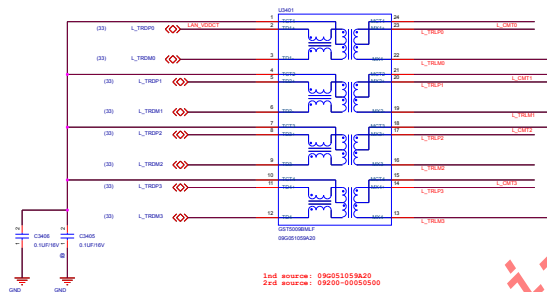
Table 17. Power Sequence Parameters

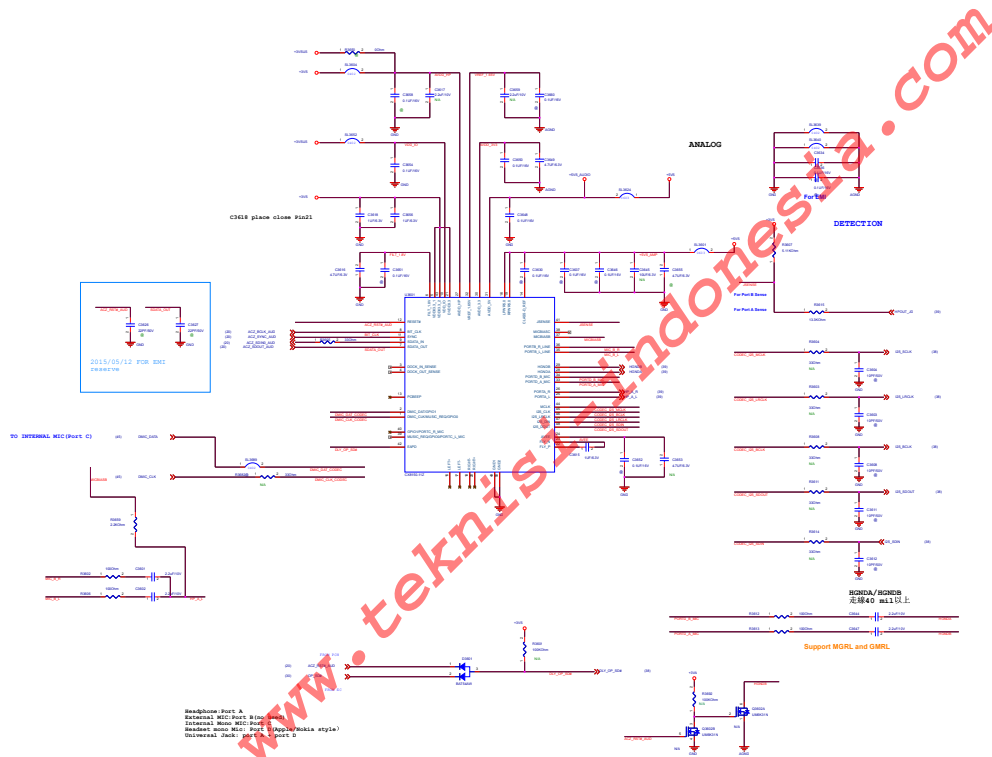
Symbol	Parameter	Min	Typical	Max	Units
W1	1.8V Rise Time	0	100	400	ns
W2	1.8V Fall Time	0	100	400	ns
W3	1.8V Hold Time	0	100	400	ns

Note: Use the following notation for power sequence parameters.

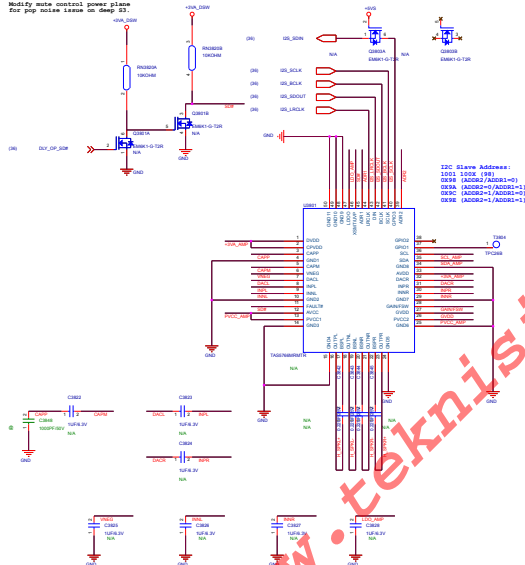


## RJ45 con.

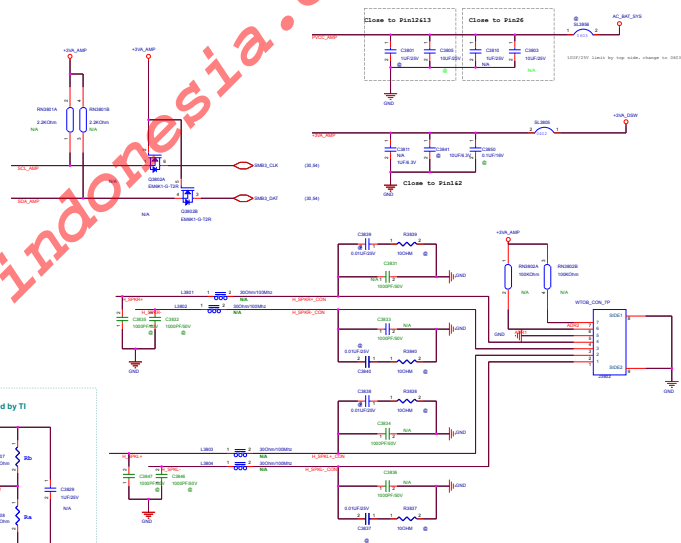
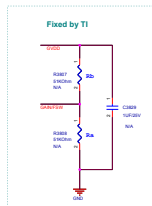




Modify mute control power plane  
for pop noise issue on deep S3.

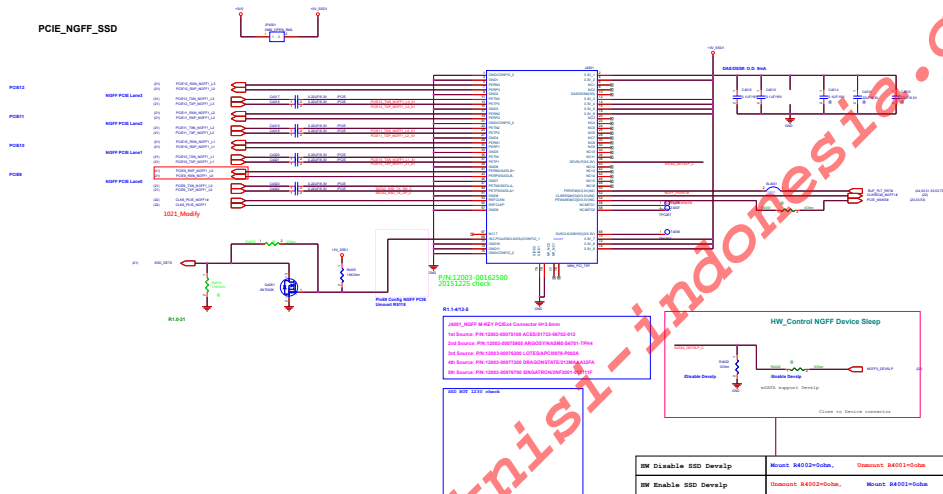


```
I2C Slave Address:
1001 100X (98)
0X98 (ADDR2=0/ADDR1=0)
0X9A (ADDR2=0/ADDR1=1)
0X9C (ADDR2=1/ADDR1=0)
0X9E (ADDR2=1/ADDR1=1)
```





# PCIe\_NGFF\_SSD



Selection Table

0x70	0x78	0x7B	0x7C	0x7D	0x7E	0x7F	0x70
1.5A	2A	2.6A	3.3A	4.2A	5.1A	6A	
8.2A	0.2A	0.8A	4.7A	2.5A	2.7A	2A	

2nd UP1905  
EE線路 for Thermal Team

ALLPDR pull low if sensed temp.  
is higher than setting

Check 其他頁是否有  
pull high 到 3.3V

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R4101	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R4102	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Selection Table

0x70	0x78	0x7B	0x7C	0x7D	0x7E	0x7F	0x70
1.5A	2A	2.6A	3.3A	4.2A	5.1A	6A	
8.2A	0.2A	0.8A	4.7A	2.5A	2.7A	2A	

2nd UP1905  
EE線路 for Thermal Team

ALLPDR pull low if sensed temp.  
is higher than setting

Check 其他頁是否有  
pull high 到 3.3V

Selection Table

0x70	0x78	0x7B	0x7C	0x7D	0x7E	0x7F	0x70
1.5A	2A	2.6A	3.3A	4.3A	5.1A	6A	
8.2A	0.2A	0.8A	4.7A	2.5A	2.7A	2A	

2nd UP1905  
EE線路 for Thermal Team

ALLPDR pull low if sensed temp.  
is higher than setting

Check 其他頁是否有  
pull high 到 3.3V

Selection Table

0x70	0x78	0x7B	0x7C	0x7D	0x7E	0x7F	0x70
1.5A	2A	2.6A	3.3A	4.2A	5.1A	6A	
8.2A	0.2A	0.8A	4.7A	2.5A	2.7A	2A	

2nd UP1905  
EE線路 for Thermal Team

ALLPDR pull low if sensed temp.  
is higher than setting

Check 其他頁是否有  
pull high 到 3.3V

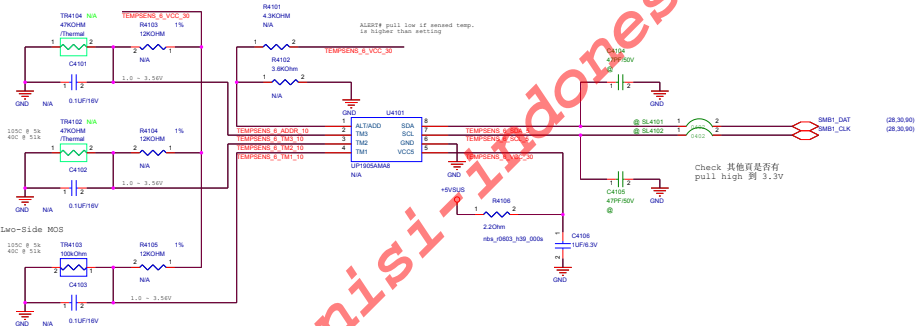
Selection Table

0x70	0x78	0x7B	0x7C	0x7D	0x7E	0x7F	0x70
1.5A	2A	2.6A	3.3A	4.3A	5.1A	6A	
8.2A	0.2A	0.8A	4.7A	2.5A	2.7A	2A	

2nd UP1905  
EE線路 for Thermal Team

ALLPDR pull low if sensed temp.  
is higher than setting

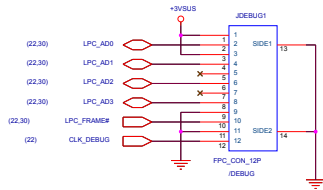
Check 其他頁是否有  
pull high 到 3.3V



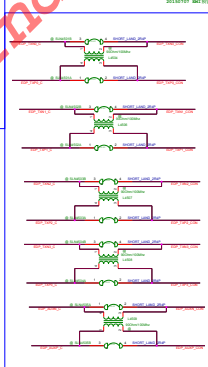
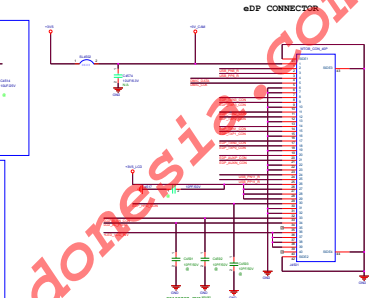
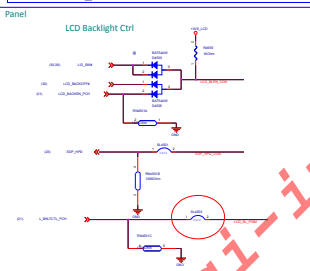
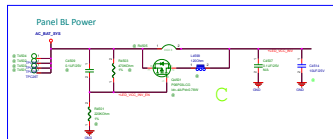
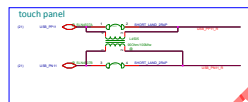
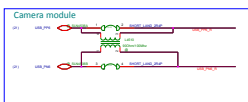
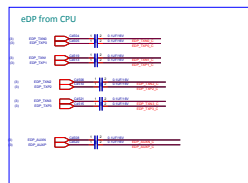
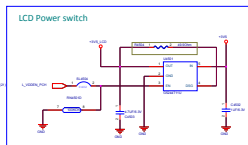
Check 其他頁是否有  
pull high 到 3.3v

(28,30,90)  
(28,30,90)

### LPC Debug Port



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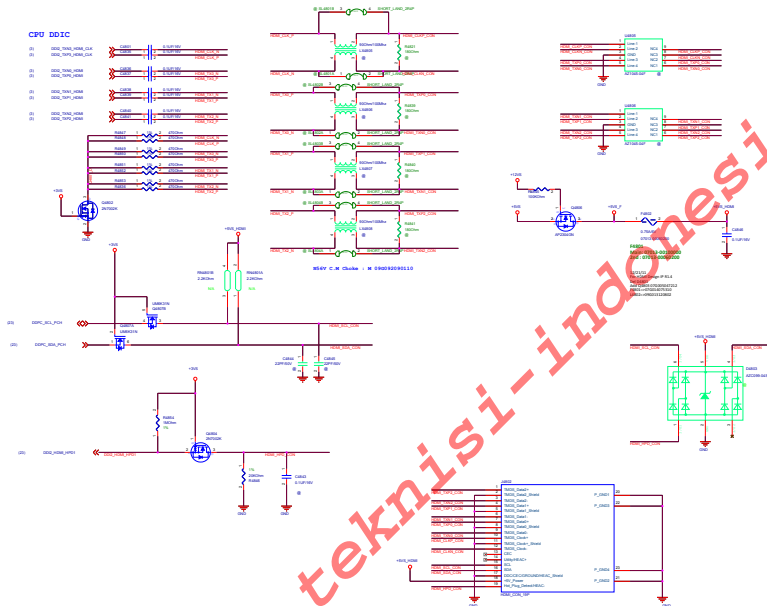
www.teknisi-indonesia.com



eDP to VGA

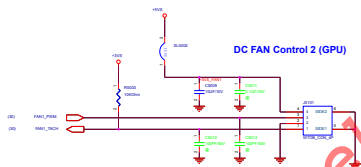
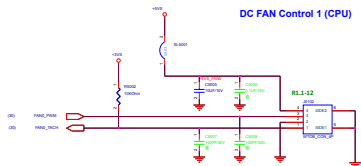
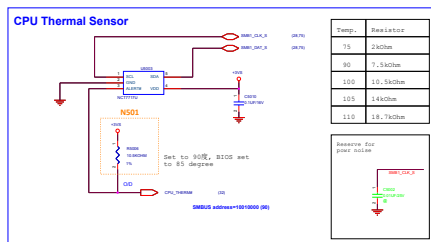
CRT D-SUB

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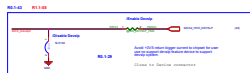
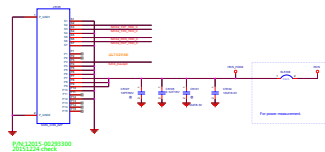


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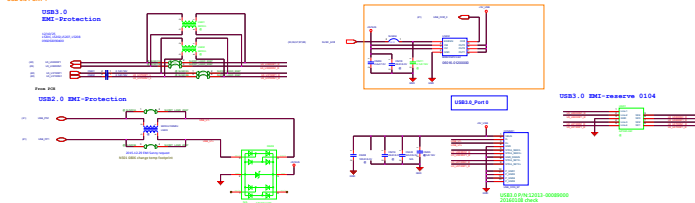


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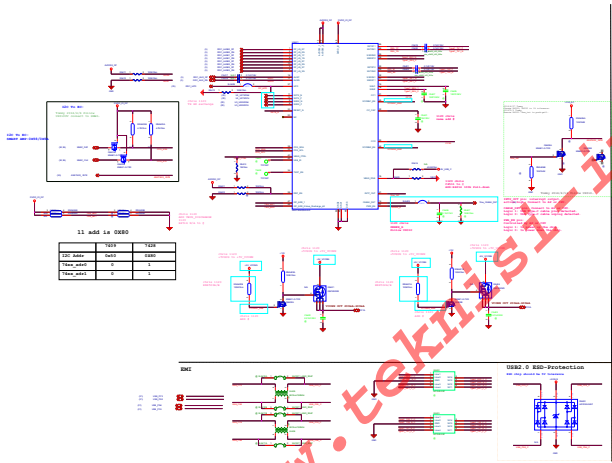
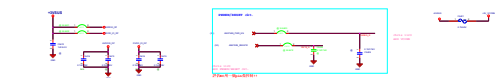
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USB 3.0 PORT 1



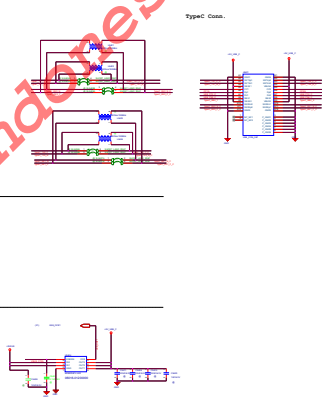
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11 add La Q880

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1000	0000	0000
1000	0000	0000
1000	0000	0000



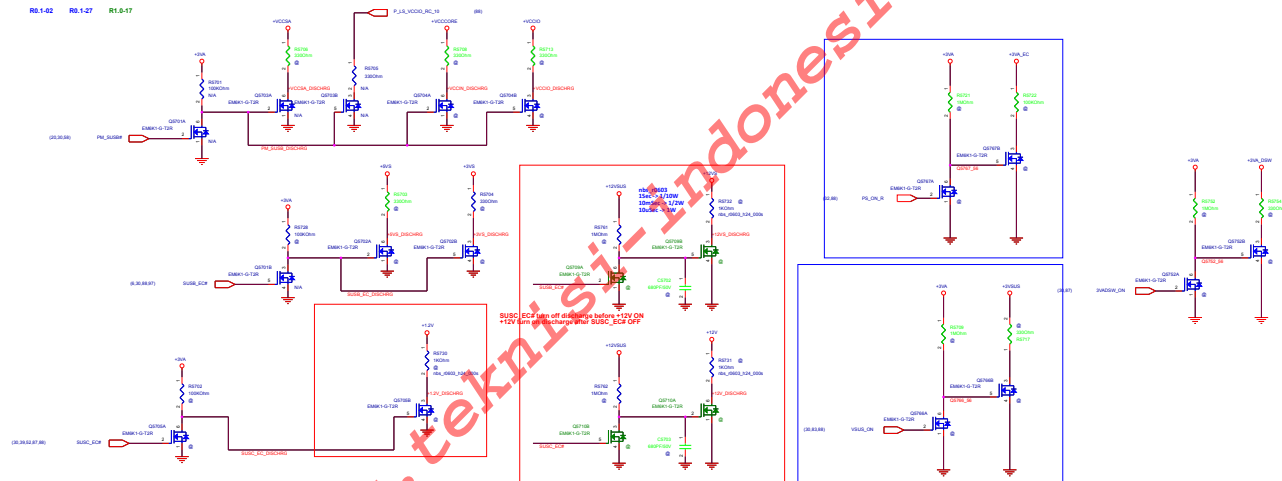
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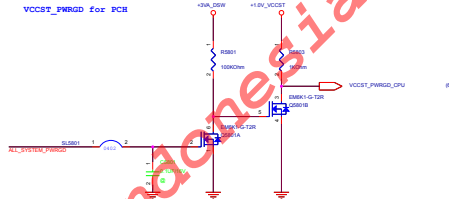
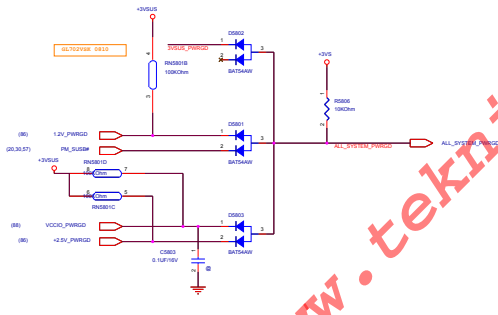
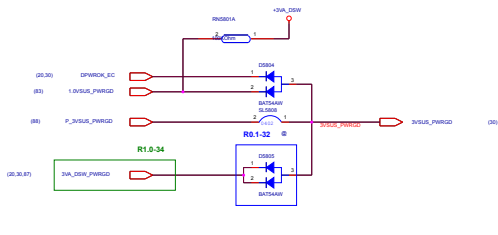
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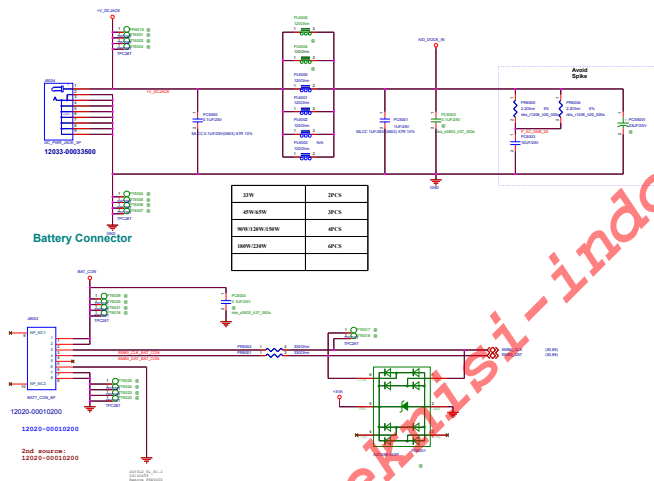
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RS-1-02 RS-1-27 RS-1-17





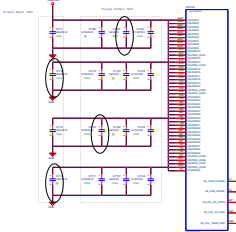
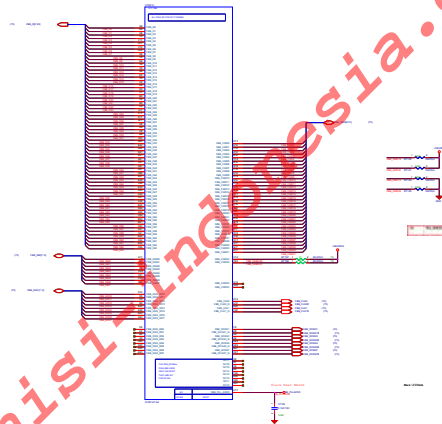
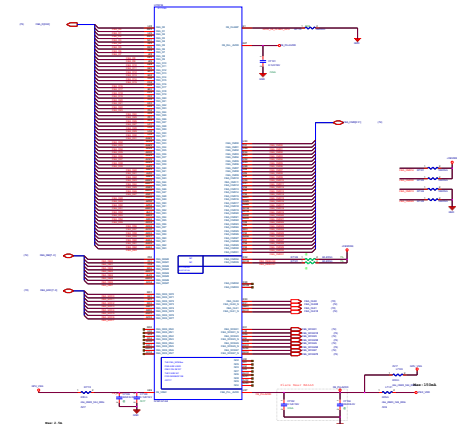
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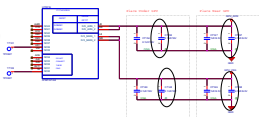


Figure 1: GPU Memory Interface: Partition A. This figure contains four detailed circuit diagrams (a, b, c, d) showing the GPU memory interface for Partition A. Diagram (a) shows the memory array and control logic. Diagram (b) shows the memory array and control logic. Diagram (c) shows the memory array and control logic. Diagram (d) shows the memory array and control logic. The diagrams include various components like memory arrays, control logic, and signal lines. A large watermark 'www.Teknisi-Indonesia.com' is overlaid diagonally across the figure.



(Table 4.16) GPU-Side FB/DDQ Decoupling Requirements

Configuration	Approx. Cost (USD)	Approx. Performance (FPS)
Core i7-10700K, RTX 3090, 32GB RAM	~\$2,500	~144 FPS
Core i7-10700K, RTX 3080, 16GB RAM	~\$1,500	~108 FPS
Core i7-10700K, RTX 3070, 16GB RAM	~\$1,000	~72 FPS
Core i7-10700K, RTX 3060, 16GB RAM	~\$700	~54 FPS
Core i7-10700K, RTX 3050, 8GB RAM	~\$400	~36 FPS



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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[illegible]

\*\* default pins are configurations  
 Please, pins are recommended for the substrate  
 The entire default pins are the assigned are tested.  
 To improve the input loading, please identify

## ME=0 Normal



CMD mapping mode H	
U64-64 G64-128*	CPU G...11
CMD0	CS#
CMD1	A0_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_AB
CMD7	A6_A11
CMD8	AB#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_AB
CMD12	RAS#
CMD13	RST#
CMD14	CXE#
CMD15	CAG#

USE GDDR6 VRAM 12GB x 32 (\$12MB)

2nd: P/N: 02008-00020000 SAMSUNG/K4G41325FC-HC4, 32Gb, 1x1 (+1.5V, non-RV)



CMD mapping mode H	
UBA-64 GBA-128*	CHI 32...63
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	AB#
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS#
CMD29	RS7#
CMD30	CXE#
CMD31	CAS#

1000

Year	1990	1991	1992	1993
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1991	1	1	1	1
1992	1	1	1	1
1993	1	1	1	1
1994	1	1	1	1
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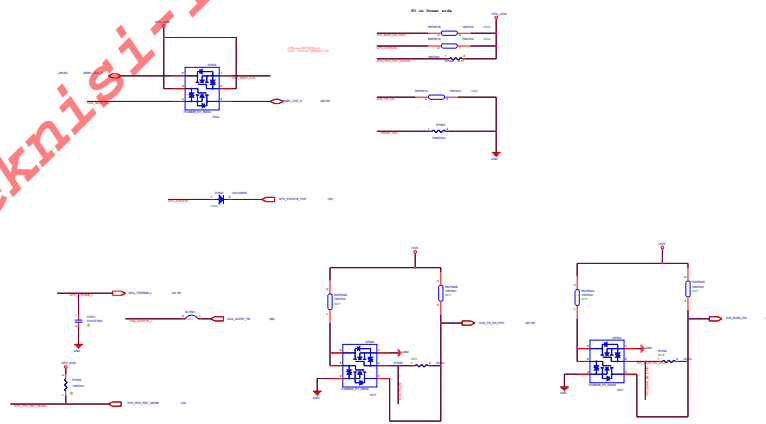
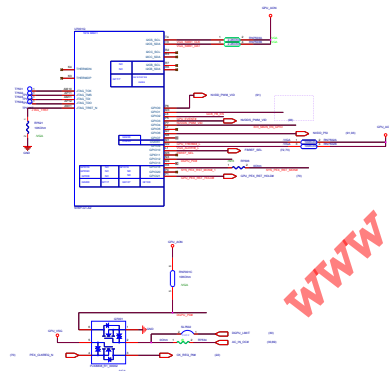




GPIO, TEMP SENSOR, JTAG  
I2C ADDRESS: 0x6Eh

Rev: G04\_2.0

GPIO Pin	M16 GPIO Function	M16 GPIO Co-Sense	M17 GPIO Function	Comments
GPIO0	SCL_P8_B4	PWR_RST	PWR_VDD	M17 PWR_RST for M16G2
GPIO1	ANAL_VDD_CTL	GCL_P8_B4	GCL_P8_B4	
GPIO2	LED_B1_PWR	GCL_INDET0	GCL_INDET0	
GPIO3	LED_VDD	WINDUP_PWR	WINDUP_PWR	M17 PWR_VDD for M16G2
GPIO4	LED_B1_B4	TVS_INDET0	TVS_INDET0	
GPIO5	TVS_INDET0	FRAME_LOCKP	FRAME_LOCKP	
GPIO6	GCL_INDET0	PS	PS	M17 PS for M16G2
GPIO7	LED_VDD	LED_B1_PWR	LED_B1_PWR	
GPIO8	TVS_P8_B1_M0	PPV_P8B	PPV_P8B	
GPIO9	THRM_ALERT	THRM_ALERT	THRM_ALERT	
GPIO10	ANAL_VREF_CTL	ANAL_VREF_CTL	ANAL_VREF_CTL	
GPIO11	PWR_VDD	LED_VDD	LED_VDD	
GPIO12	PWR_VDD	PWR_VDD	PWR_VDD	
GPIO13	PS	LED_B1_PWR	LED_B1_PWR	
GPIO14	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO15	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO16	FRAME_LOCKP	FRAME_LOCKP	FRAME_LOCKP	
GPIO17	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO18	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO19	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO20	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO21	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO22	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO23	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO24	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO25	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO26	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO27	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO28	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
GPIO29	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	
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GPIO31	WINDUP_PWR	WINDUP_PWR	WINDUP_PWR	



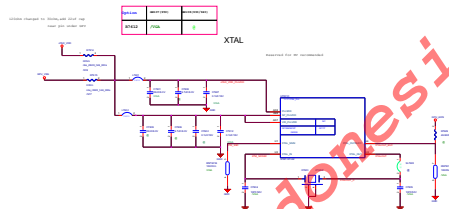
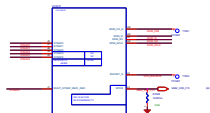


Table 3. B179 G6/G1 G6G5 Recommended Memories

Memory Type	Memory Configuration	Memory Vendor	Manufacturer Part Number	Die Revision	Memory Size	Memory Speed Grade	Memory Temp. Range	Qual. Pkg.	Status
B1A	256Kx16	Micron	MT19LC16040AF-10-A	0-00	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-01	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-02	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-03	16Kb	7.0ns	0 to 70°C	Full	Production ready
B1A	128Kx16	Micron	MT19LC16040AF-10-A	0-00	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-01	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-02	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-03	16Kb	7.0ns	0 to 70°C	Full	Production ready

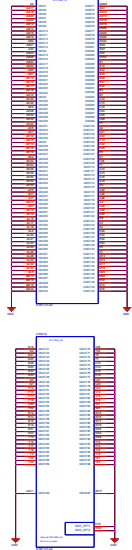
Note:  
1. For B179G6, the maximum allowable memory case temperature is 85°C.  
2. B179G6 is supported in 32-bit configuration only.

Table 7. B179 G6/G1 G6G5 Recommended Memories

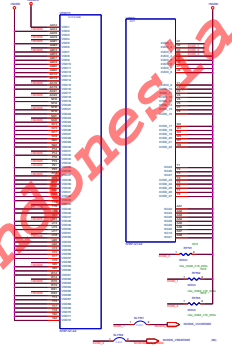
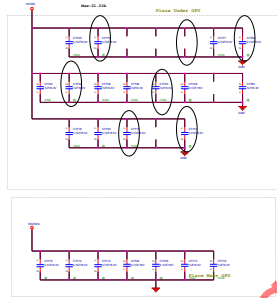
Memory Type	Memory Configuration	Memory Vendor	Manufacturer Part Number	Die Revision	Memory Size	Memory Speed Grade	Memory Temp. Range	Qual. Pkg.	Status
B1A	256Kx16	Micron	MT19LC16040AF-10-A	0-00	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-01	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-02	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-03	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-04	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-05	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-06	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-07	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-08	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-09	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-10	16Kb	7.0ns	0 to 70°C	Full	Production ready
			MT19LC16040AF-10-A	0-11	16Kb	7.0ns	0 to 70°C	Full	Production ready

Note:  
1. For B179G6/G1, the maximum allowable memory case temperature is 85°C.  
2. B179G6 is supported in 32-bit configuration only.

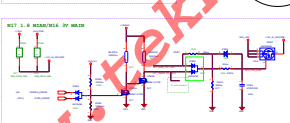
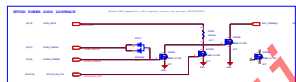
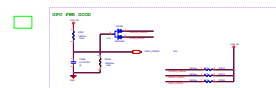
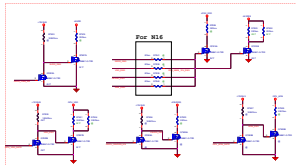
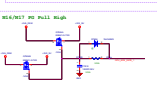
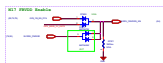
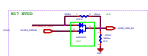
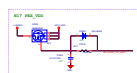
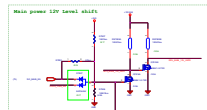
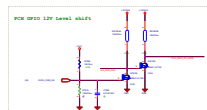
### NVDD GROUND



### NVDD POWER AND DECOUPLING

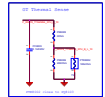
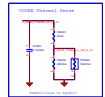
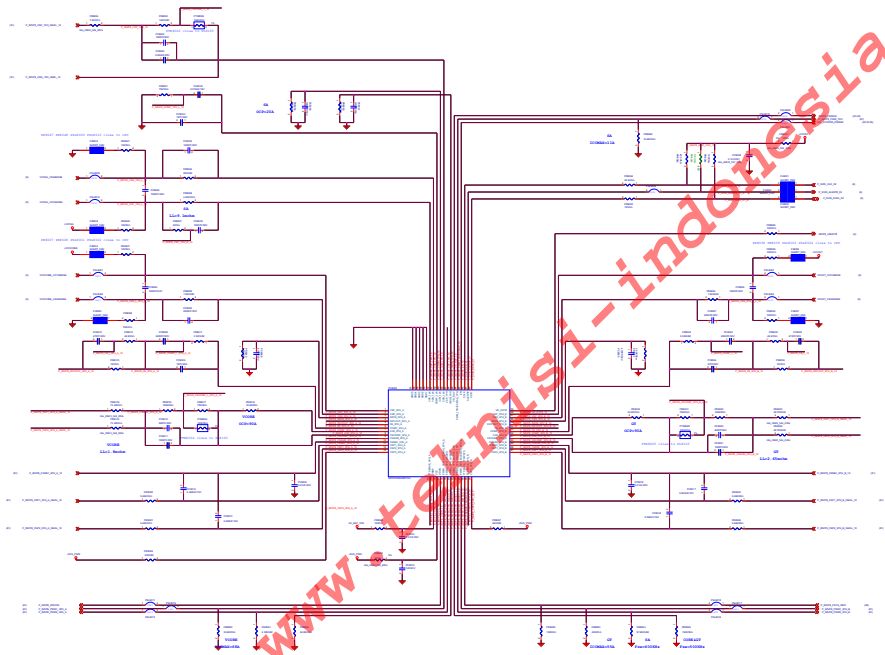


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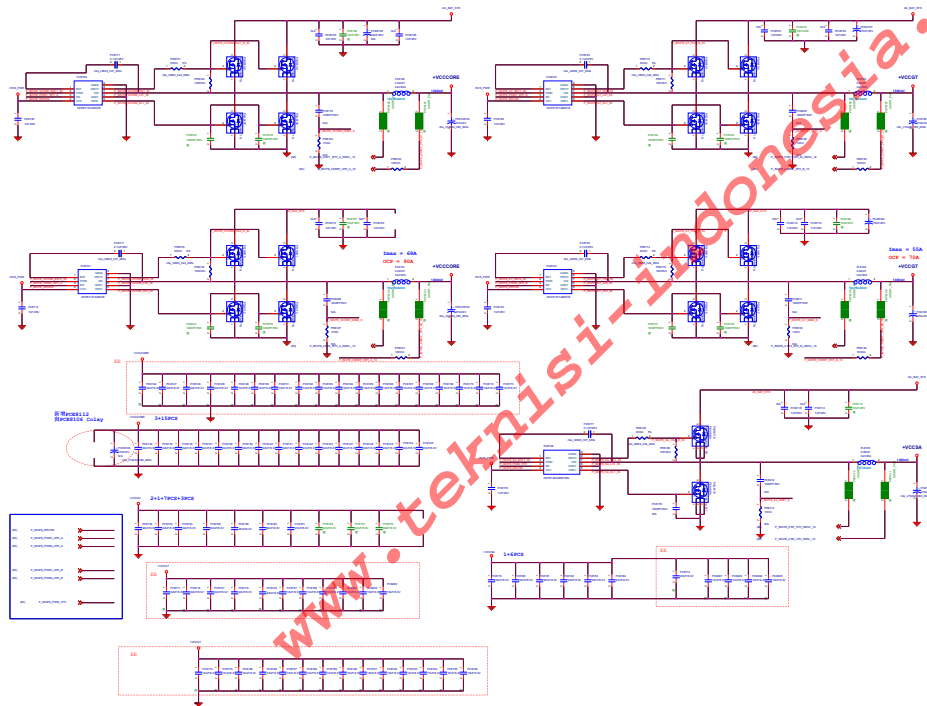


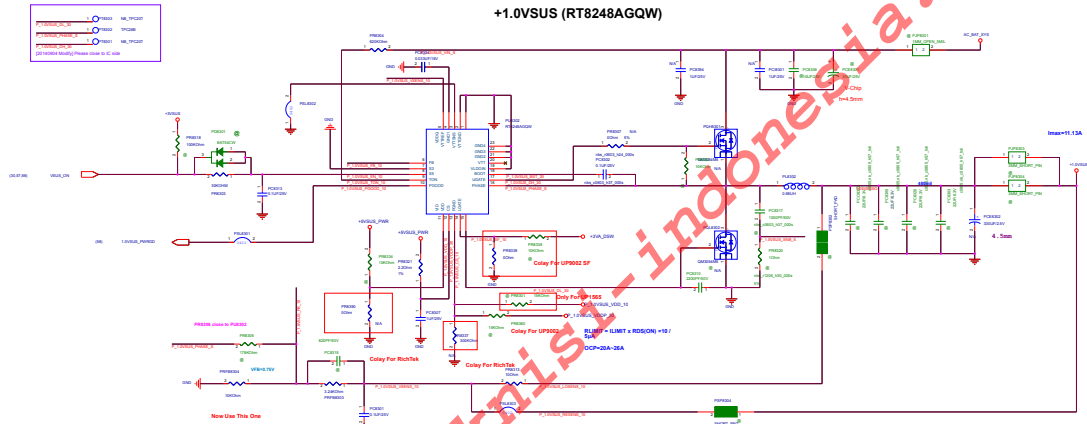
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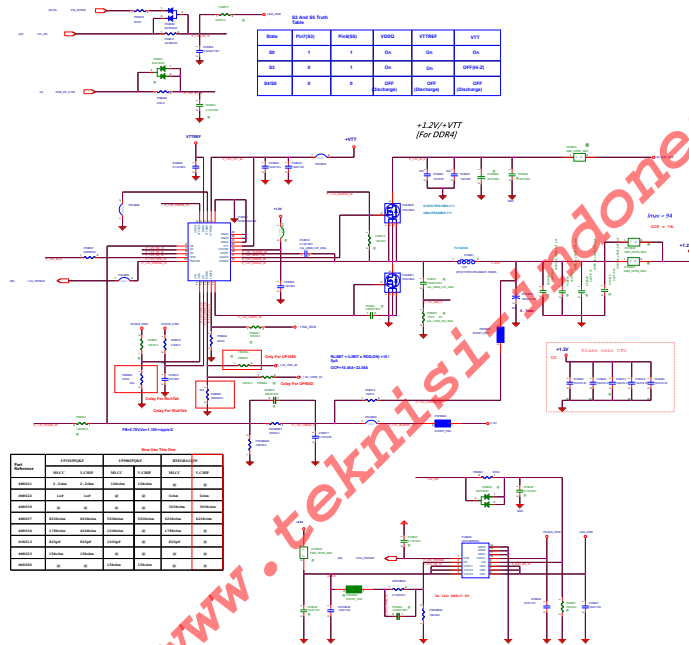
Kabelake IMVP8 Power (For CPU)



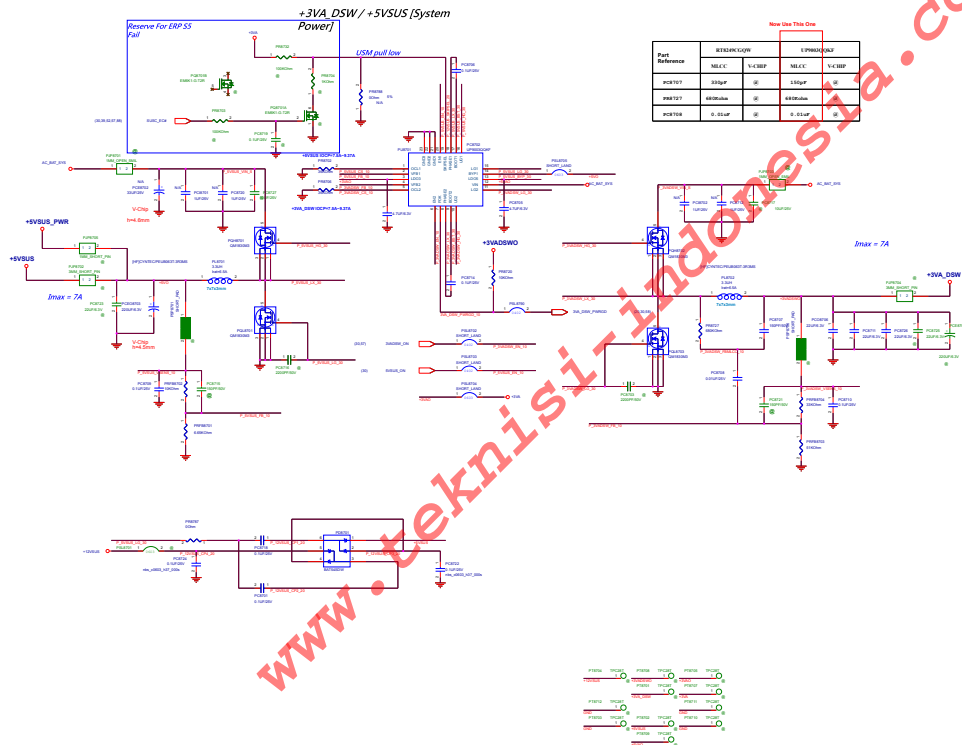


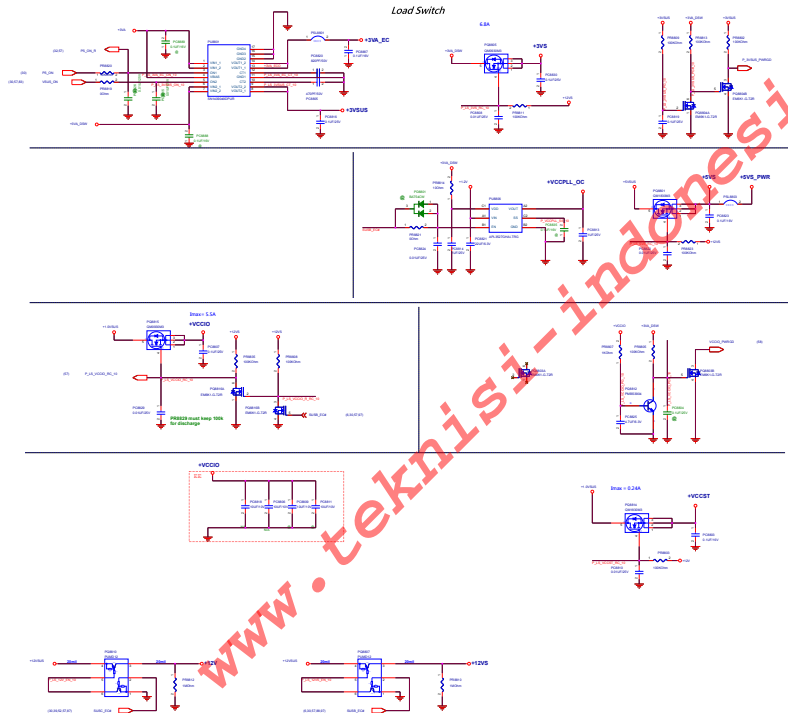
**Now Use This One**

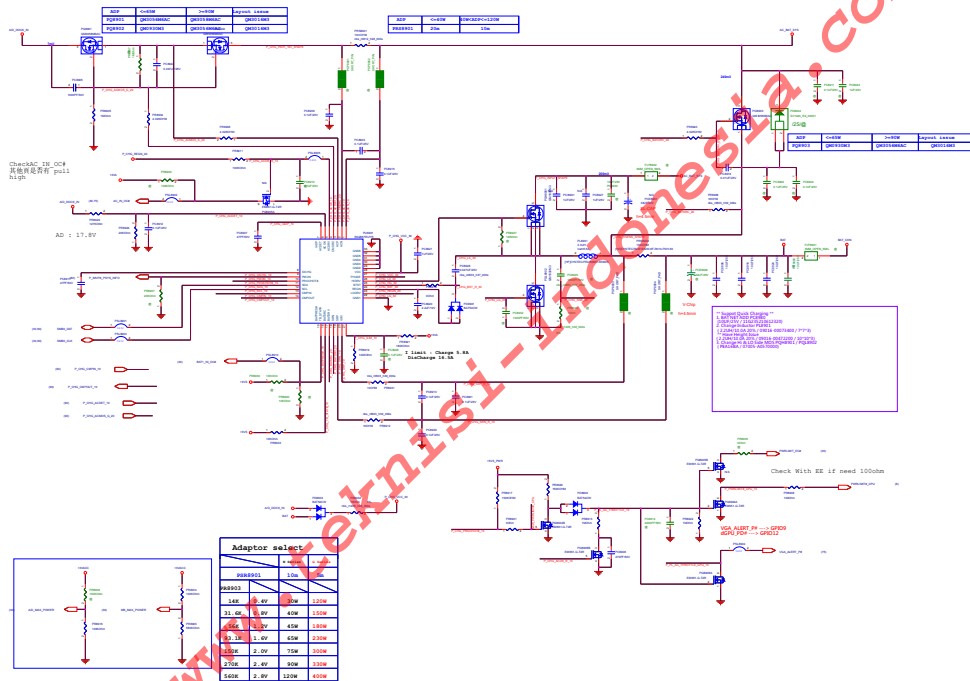
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PWR019	1uF	1uF	Ω	Ω	Ω	Ω
PWR017	Ω	Ω	Ω	Ω	3000uohm	3000uohm
PWR004	8200uohm	8200uohm	5400uohm	5400uohm	4200uohm	4200uohm
PWR006	1700uohm	4020uohm	1.000uohm	Ω	1700uohm	Ω
PWR015	820pF	820pF	1.000pF	Ω	820pF	Ω
PWR001	100uohm	100uohm	Ω	Ω	Ω	Ω
PWR000	Ω	Ω	100uohm	100uohm	Ω	Ω





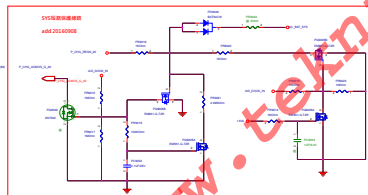
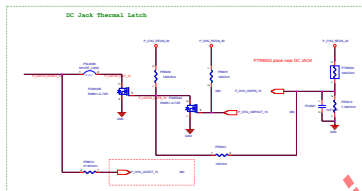
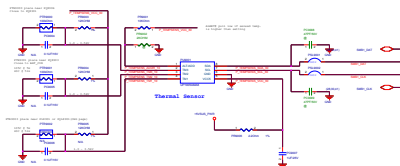




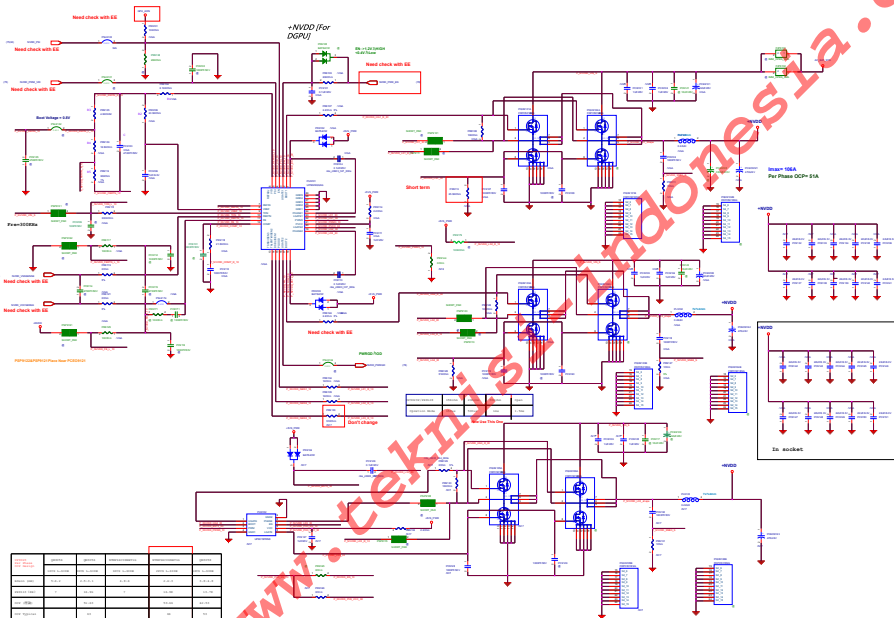


Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	0	0	0	0	0	0	0	0
0x01	0	0	0	0	0	0	1	0
0x02	0	0	0	0	0	1	0	0
0x03	0	0	0	0	0	1	1	0
0x04	0	0	0	0	1	0	0	0
0x05	0	0	0	0	1	0	1	0
0x06	0	0	0	0	1	1	0	0
0x07	0	0	0	0	1	1	1	0
0x08	0	0	0	1	0	0	0	0
0x09	0	0	0	1	0	0	1	0
0x0A	0	0	0	1	0	1	0	0
0x0B	0	0	0	1	0	1	1	0
0x0C	0	0	0	1	1	0	0	0
0x0D	0	0	0	1	1	0	1	0
0x0E	0	0	0	1	1	1	0	0
0x0F	0	0	0	1	1	1	1	0

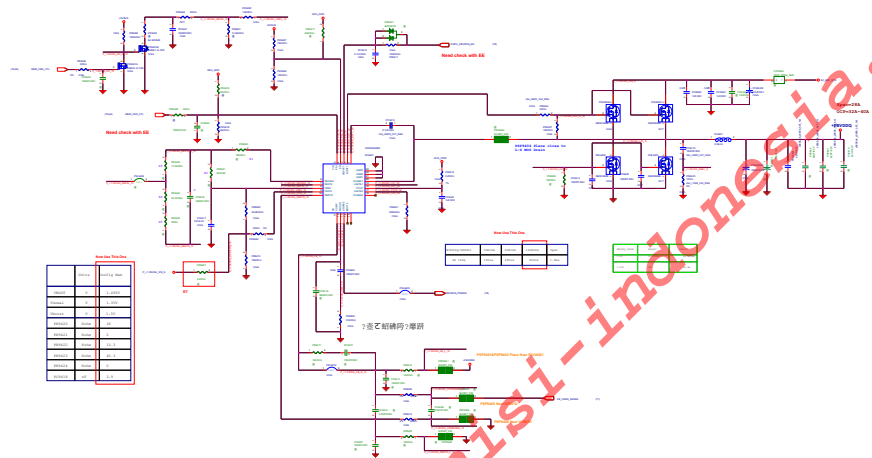
Register Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	0	0	0	0	0	0	0	0
0x01	0	0	0	0	0	0	1	0
0x02	0	0	0	0	0	1	0	0
0x03	0	0	0	0	0	1	1	0
0x04	0	0	0	1	0	0	0	0
0x05	0	0	0	1	0	0	1	0
0x06	0	0	0	1	0	1	0	0
0x07	0	0	0	1	0	1	1	0
0x08	0	0	1	0	0	0	0	0
0x09	0	0	1	0	0	0	1	0
0x0A	0	0	1	0	0	1	0	0
0x0B	0	0	1	0	0	1	1	0
0x0C	0	0	1	1	0	0	0	0
0x0D	0	0	1	1	0	0	1	0
0x0E	0	0	1	1	0	1	0	0
0x0F	0	0	1	1	0	1	1	0



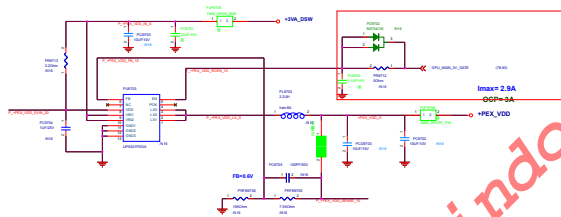
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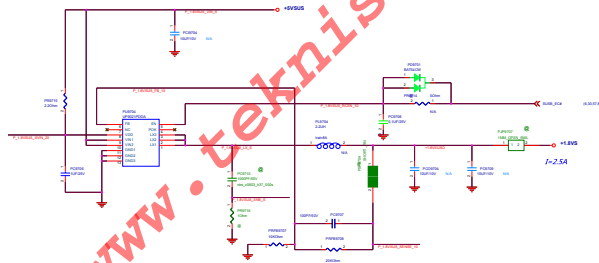




## N17 POWER quence

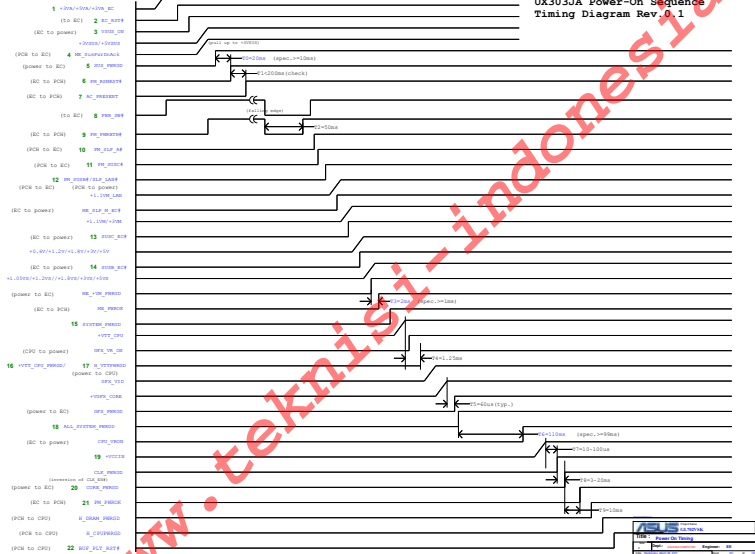


+1.8VS [For PCH]







UX303JA Power-On Sequence  
Timing Diagram Rev.0.1

[illegible]